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EXAMINER	
KAWSAR, ABDULLAH AL	
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2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/573,918	LESCOUET ET AL.
	Examiner	Art Unit
	ABDULLAH AL KAWSAR	2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 6-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 6-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2011* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/30/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3, 6-32 are pending.

Claim Objections

2. Claim 31 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple independent claims. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

3. Claim 3 is objected to because of the following informalities:

a. Claim 3 is dependent on canceled claim 2. For examination purpose examiner interprets claim 2 dependent on claim 1.

b. Claim 8, line 2 recites "common program is operable" wherein operable is definite to perform the function as defined in the claimed limitation. Applicant is suggested to replace "operable" with "executed".

Appropriate correction required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 6-7, 11-22, 26-31 rejected under 35 U.S.C. 103(a) as being unpatentable over Ohno et al.(US Patent No. 6,715, 016), in view of Sekiguchi et al. (US Patent Publication No. 2001/0016879).

5. Sekiguchi was cited in the IDS filed on 12/30/2010.

6. As per claim 1, Ohno teaches the invention as claimed including a method of enabling multiple different operating systems to run concurrently on the same computer (figure 1), comprising:

selecting a first operating system to have a high priority (col 3, lines 53-55; OS-B);

selecting at least one second operating system to have a lower priority (col 3, lines 39-42; lines 53-57; OS-A);

providing a common program arranged to switch between said operating systems under predetermined conditions (col 3, lines 59-65); and

providing modifications to said first and second operating systems to allow them to be controlled by said common program (col 1, lines 64-67 through col 2, lines 1-19).

wherein switching between said operating systems includes invoking the common program by calling an exception vector (col 3, lines 59-65), and

Ohno does not specifically disclose wherein calling an exception vector to invoke the common program simulates an exception caused by an external event.

However Sekiguchi teaches wherein calling an exception vector to invoke the common program(interrupt management program) simulates (virtual address for each interrupt) an exception caused by an external event (par. 0057; par. 0072; par. 0158; external interrupts are

simulated by mapping with the virtual address and invoking the interrupt management program to perform the interrupt function from the interrupt table based on the virtual address).

7. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Sekiguchi into the method of Ohno to call and exception vector for invoking the common program simulates an exception caused by an external event. The modification would have been obvious because one of the ordinary skills of the art would be motivated to utilize the teaching of Sekiguchi to simulate the external interrupt events to invoke the interrupt management program for performing the interrupt function with the proper operating system that the interrupt is intended for based on the virtual address mapping with the interrupt number for faster interrupt service.

8. As per claim 3, Ohno teaches allocating exception vectors to trap calls, thereby to enable invocation of the common program using a trap call mechanism (col 3, lines 59-67 through col 4, lines 1-2).

9. As per claim 6, Ohno teaches wherein the common program preempts the first or second operating system by intercepting exception or interrupt vectors (col 7, lines 21-54).

10. As per claim 7, Ohno teaches using a exception handler table containing an array of pointers to intercept exceptions, and activating an exception handler program to preempt the first or second operating system (col 4,lines 38-41).

11. As per claim 11, Sekiguchi teaches enabling hardware interrupts throughout the operation of the second operating system except during the operation of subroutines that save machine state (figure 16; OS switch is initiated and the context is stored before performing any other operation and no other operation is performed before and during the OS context is stored that will include any interrupts).

12. As per claim 12, Ohno teaches in which the first operating system is a real time operating system (col 3, lines 53-55).

13. As per claim 13, Ohno teaches in which the second operating system is a non-real time, general-purpose operating system (col 3, lines 39-42).

14. As per claim 14, Ohno teaches in which the second operating system is Linux, or a version or variant thereof (col 3, lines 39-42).

15. As per claim 15, Ohno teaches in which the common program is arranged to save, and to restore from a saved version, the processor state required to switch between the operating systems (col 2, lines 4-11).

16. As per claim 16, Ohno teaches in which processor exceptions for the second operating system are handled in virtual fashion by the common program (col 8, lines 41-45).

17. As per claim 17, Ohno teaches in which the common program is arranged to intercept some processor exceptions, and to call exception handling routines of the first operating system to service them (col 7, lines 21-41).

18. As per claim 18, Ohno teaches in which the processor exceptions for the second operating system are notified as virtual exceptions (col 8, lines 33-49).

19. As per claim 19, Ohno teaches in which the common program is arranged to call an exception handling routine of the second operating system corresponding to a said virtual exception which is pending (col 8, lines 33-49).

20. As per claim 20, Ohno teaches further comprising providing each of said operating systems with separate memory spaces in which each can exclusively operate (col 4, lines 65-67 through col 5, lines 1-2).

21. As per claim 21, Ohno teaches further comprising providing each of said operating systems with first input and/or output devices of said computer to which each has exclusive access (col 3, lines 24-28; col 4, lines 38-46).

22. As per claim 22, Ohno teaches in which each operating system accesses said first input and/or output devices using substantially unmodified native routines (col 4, lines 58-64).

23. As per claim 26, Ohno teaches combining said operating systems and common program into a single code product (col 1, lines 64-67 through col 2, lines 1-4).

24. As per claim 27, Ohno teaches embedding said operating systems and common program onto persistent memory on a computer product (col 2, lines 20-23).

25. As per claim 28, Ohno teaches a development kit computer program product comprising code for performing the steps of claim 1 (col 2, lines 20-23).

26. As per claim 29, Ohno teaches a computer program product comprising code combined according to claim 36 (col 1, lines 64-67 through col 2, lines 1-4).

27. As per claim 30, Ohno teaches the invention as claimed including a computer system comprising:

a CPU, memory devices and input/output devices, said CPU being arranged to execute (col 2, lines 57-65; figure 1), computer code comprising:

a first operating system having a relatively high priority (col 3, lines 53-55);

a second operating system having a relatively lower priority (col 3, lines 39-42; lines 53-57); and

a common program arranged to run said operating systems concurrently by switching between said operating systems under predetermined conditions (col 3, lines 59-65),

wherein switching between said operating systems includes the first or second operating system invoking the common program by calling an exception vector (col 3, lines 59-65),

Ohno does not specifically disclose wherein an exception vector to invoke the common program simulates an exception caused by an external event.

However Sekiguchi teaches wherein an exception vector to invoke the common program simulates an exception caused by an external event (par. 0057; par. 0072; par. 0158; external interrupts are simulated by mapping with the virtual address and invoking the interrupt management program to perform the interrupt function from the interrupt table based on the virtual address).

28. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Sekiguchi into the method of Ohno to call and exception vector for invoking the common program simulates an exception caused by an external event. The modification would have been obvious because one of the ordinary skills of the art would be motivated to utilize the teaching of Sekiguchi to simulate the external interrupt events to invoke the interrupt management program for performing the interrupt function with the proper operating system that the interrupt is intended for based on the virtual address mapping with the interrupt number for faster interrupt service.

29. As per claim 31, Ohno teaches a computer system according to claim 28, arranged to run said first and second operating systems concurrently using the method as described above (col 3, lines 39-52).

30. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohno et al.(US Patent No. 6,715,016), Sekiguchi et al. (US Patent Publication No. 2001/0016879), as applied to claim 1 and 30, in view of Blanset et al.(US Patent No. 4,747,040).

31. As per claim 8, Ohno and Sekiguchi do not specifically disclose teaches wherein the common program is operable in real mode in physical processor address space(col 3, lines 53-67 through col 4, lines 1-6; Ohno).

However Blanset teaches wherein the common program is operable in real mode in physical processor address space (col 4, lines 36-41; col 8, lines 12-67)

32. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Blanset into the combined method of Ohno and Sekiguchi to have the common program operable in real mode. The modification would have been obvious because one of the ordinary skills of the art would be motivated to utilize the teaching of Blanset to operate the common program in real mode to have real memory access to the physical memory without simulating the memory address mapping for better system execution control.

33. As per claim 9, Blanset teaches preempting the first or second operating system by the common program, and switching to real mode in physical processor address space when

preempting the first or second operating system (col 8, lines 12-67; col 12, lines 64-68 through col 13, lines 1-12).

34. As per claim 10, Blanset teaches invoking the common program by the first or second operating system, and switching to real mode in physical processor address space when invoking the common program (col 8, lines 12-67; col 12, lines 64-68 through col 13, lines 1-12).

35. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohno et al.(US Patent No. 6,715,016), Sekiguchi et al. (US Patent Publication No. 2001/0016879), as applied to claim 1 and 30, in view of Endo et al.(US Patent No. 6,615,303).

36. As per claim 23, Ohno and Sekiguchi do not specifically disclose providing each of said operating systems with access to second input and/or output devices of said computer to which each has shared access.

However Endo teaches providing each of said operating systems with access to second input and/or output devices of said computer to which each has shared access (figure 11, element 192).

37. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Endo into the method of Ohno to have shared access to input and output devices from both operating system. The modification would have been obvious because one of the ordinary skills of the art would be motivated to utilize the teaching of Endo to

have shared access to input/output devices from both operating systems for using the functionality of the input/output devices from both operating systems.

38. As per claim 24, Endo teaches in which all operating systems access said second input and/or output devices using the routines of the first operating system (col 12, lines 63-67).

39. As per claim 25, Ohno teaches in which the common program provides trap call mechanisms, to control the operation of the second operating system, and/or event mechanisms to notify the first operating system of status changes in the second operating system (col 7, lines 55-60).

40. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohno et al.(US Patent No. 6,715,016), Sekiguchi et al. (US Patent Publication No. 2001/0016879), as applied to claim 1 and 30, and in view of Cota-Robles(US PGPUB 2003/0037089).

41. As per claim 32, Ohno and Sekiguchi do not specifically disclose in which the computer has a Reduced Instruction Set architecture.

However Cota-Robles teaches in which the computer has a Reduced Instruction Set architecture (par. 0042).

42. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Cota-Robles into the combined method of Ohno and

Sekiguchi to have the computer with reduced instruction set architecture. The modification would have been obvious because one of the ordinary skills of the art would be motivated to utilize the teaching of Cota-Robles to have reduced architecture set for executing the applications with better memory management.

Response to Arguments

Applicant's arguments with respect to claim(s) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on Monday to Thursday between 8:00am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Abdullah-Al Kawsar/
Examiner, Art Unit 2195

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